REMARKS

Claim Objections

In the Office Action, claims 14 and 16 are objected to for formal reasons. The foregoing amendments to claim 14 address the concerns of the Examiner. Therefore, the objection to claims 14 and 16 should be withdrawn.

Claim Rejections 35 U.S.C. § 102

Rejections on Lin

Claims 1-7, 12 and 13 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 6,850,440 to Lin et al. (hereafter "Lin"). This rejection is respectfully traversed.

Claim 1, as amended, recites:

> A method for programming a single bit nonvolatile memory cell integrated on a metal-dielectric-semiconductor technology chip, the memory cell comprising a semiconductor substrate including a source, a drain, and a channel in-between the source and the drain; and a control gate that comprises a control gate electrode and a dielectric stack, the control gate electrode being separated from the channel by the dielectric stack, the dielectric stack comprising at least one charge storage dielectric layer, wherein the method for programming comprises:
>
> applying electrical ground to the source;
>
> applying a first voltage having a first polarity to the drain;
>
> applying a second voltage of the first polarity to the control gate electrode; and
>
> applying a third voltage having a second polarity opposite to the first polarity to the semiconductor substrate,
>
> wherein the first, second and third voltages cooperatively effect programming of the memory cell as a result of injection of hot carriers from the drain of the memory cell, the hot carriers being (i) generated by a secondary impact ionization mechanism (ii) injected into the at least one charge storage dielectric layer and (iii) stored on the at least one charge storage dielectric layer.

Claim 1 is directed to a method for programming a single bit nonvolatile memory cell that is integrated on a metal-dielectric-semiconductor technology chip. In the method, hot electrons are

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generated by a secondary impact ionization mechanism. The hot carriers are injected into and stored on at least one charge storage dielectric layer from a drain side of the memory cell, where the at least one charge storage dielectric layer is included in a dielectric stack of a control gate. One embodiment of such a memory cell 1 is illustrated in Figure 1 of the application, which is included below for the Examiner's convenience.

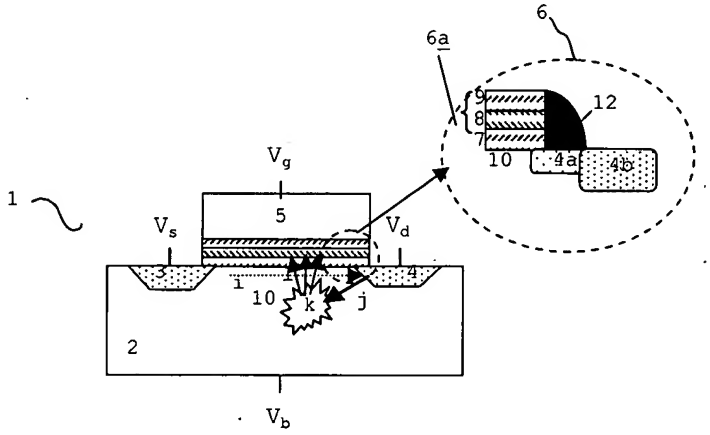

Figure 1

The memory cell 1 includes a control gate that comprises a control gate electrode 5 (which is a conductive layer – *See* application, page 11, line 23) and a dielectric stack 6a. The dielectric stack 6a includes three separate dielectric layers 7,8,9. The dielectric stack 6a shown in Figure 1 is described in the specification on page 13, line 12 through page 14, line 5, which recites:

> The stack 6a of the dielectric layers 7, 8 and 9 may be formed by depositing the first dielectric layer 7 on top of a major surface of the semiconductor substrate 2. The first dielectric layer 7 typically comprises silicon dioxide formed by thermal oxidation of the silicon substrate 2, or can be deposited by a variety of chemical vapor deposition (CVD) techniques. Alternatively, a tetra-ethoxy-silane (TEOS) layer formed by Low Pressure CVD, or oxides formed by Atomic Layer CVD) may be employed. The thickness of the first dielectric layer 7 may be between 3nm and 20 nm, or between 3nm and 10nm. The second dielectric layer 8 is formed on top of the first dielectric 7, which electrically insulates the second dielectric 8 from the channel 10 underneath. For this particular embodiment, the second dielectric layer 8 comprises a silicon nitride layer with a thickness between 2 and 20 nm, or between 5 and 12nm. The third dielectric layer 9 is formed on top of the second dielectric layer 8, e.g. by CVD, which electrically insulates the second dielectric layer 8 from the gate 5. For this

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embodiment, the third dielectric layer 9 comprises a silicon oxide having a thickness between 3 and 20 nm, or between 3 and 10nm. Such a dielectric layer stack forms an ONO (oxide-nitride-oxide) stack. For this ONO stack, the second dielectric layer 8 (nitride layer) retains the charge used for programming the memory cell 1.

The foregoing portion of the specification describes the memory cell 1 as including an ONO dielectric stack, where a nitride (silicon-nitride) layer 8 of the ONO stack acts as a charge storage dielectric layer. For the memory cell 1, hot carriers are injected into, and stored on the nitride layer 8 to effect programming of the memory cell 1.

In contrast to claim 1, Lin discloses floating gate memory cells, such as a memory cell 500, which is illustrated in Figure 5 of Lin. Figure 5 of Lin is included below for the Examiner's convenience.

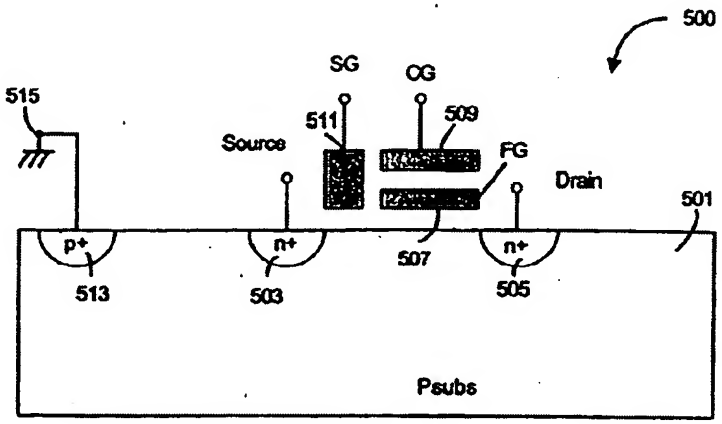

FIG. 5

The memory cell 500 shown in Figure 5 includes a floating gate 507, which is part of a split gate structure. The floating gate 507 is disposed under a control gate 509, which is a typical arrangement for floating gate nonvolatile memory cells. The split gate structure (including the floating gate 507) of the memory cell 500 is described in column 6, line 29-37 of Lin, which recites:

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> The split gate structure includes among other elements a floating gate 507, which is overlying a layer of dielectric material overlying a channel region in the substrate. The dielectric layer can be any suitable material such as high quality silicon dioxide, silicon nitride, a combination thereof, and others. In the present embodiment, the channel region has a length of about 0.6 micron and less. Alternatively, the channel length can be about 1.0 micron and less. The floating gate is often made of a suitable conductive material such as doped polysilicon and others.

The split gate structure of the memory cell 500 is further described in column 6, lines 38-49, which recites:

> A control gate 509 is defined overlying the floating gate. The control gate layer is made by a suitable conducting material such as doped polysilicon and others. The control gate layer can also have an overlying refractory metal layer, which can improve conductivity. The control gate and floating gate often have a dielectric layer or layers sandwiched in between these layers. As merely an example, the dielectric layers are often an oxide layer, a nitride layer overlying the oxide layer, and a nitride layer overlying the oxide layer, which forms a sandwiched layer commonly called "ONO." Other types of layer can also be used, however.

Lin states (column 5, line 66 through column 6, line 13) that the programming methods of his invention can be applied to memory cell 500. Such a programming method is described in column 3, lines 45-46, which recites that programming occurs as a result of "hot electrons [being] injected into the polysilicon (poly 1) floating gate." Therefore, the memory cell 500 illustrated above is programmed by hot electrons being injected into, and stored on the conductive floating gate 507.

In contrast with the approach disclosed in Lin, claim 1 recites programming a nonvolatile memory cell by injecting hot carriers into at least one charge storage dielectric layer and storing (e.g., at least some of) the injected hot carriers on the at least one charge storage dielectric layer. Therefore, Lin does not anticipate claim 1, as that patent does not disclose each an every element of claim 1. A method for programming a memory cell that includes injecting hot carriers into a conductive floating gate and storing the injected carriers on the floating gate (Lin) does not

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disclose a method of programming a memory cell that includes injecting hot carriers into at least one charge storage dielectric layer and storing those injected hot carriers on the at least one charge storage dielectric layer (claim 1). Therefore, the rejection of claim 1 should be withdrawn.

Without addressing the merits of the comments made in the Office Action with respect to claims 2-7, which are not specifically conceded, it is noted that these claims depend from claim 1 and include all of its limitations and the limitations of any intervening claims. The arguments made above with respect to claim 1 apply equally to claims 2-7 and are herein incorporated. Therefore, claims 2-7 are allowable over Lin on the same basis as claim 1 by virtue of claim dependency, and the rejection should be withdrawn.

Claim 12, as amended, recites:

> A memory circuit comprising:
> an array of single bit nonvolatile memory cells, each of the memory cells comprising a semiconductor substrate including a source, a drain, and a channel in-between the source and the drain; and a control gate that comprises a control gate electrode and a dielectric stack, the control gate electrode being separated from the channel by the dielectric stack, the dielectric stack comprising at least one charge storage dielectric layer; and
> peripheral circuitry, the peripheral circuitry coupled with the memory cell such that programming of each memory cell is effected using voltages having absolute values of 5 V or less,
> wherein the memory cells are programmed as a result of injection of hot carriers from the drain of the memory cell, at least some of the hot carriers being (i) generated by a secondary impact ionization mechanism, (ii) injected into the at least one charge storage dielectric layer and (iii) stored on the at least one charge storage dielectric layer.

Claim 12 is directed to a memory circuit that includes an array of memory cells, where the memory cells are programmed in substantially similar fashion as was described above with respect to claim 1. Claim 12 is not anticipated by Lin because Lin discloses floating gate

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memory circuits that are programmed by injecting hot carriers into a conductive floating gate electrode and storing the hot carriers on the floating gate electrode. In contrast, claim 12 recites a memory circuit that includes memory cells that are programmed by injecting hot carriers into at least one charge storage dielectric layer and storing those injected hot carriers on the at least one charge storage dielectric layer. Thus, claim 12 is not anticipated by Lin as that patent does not disclose or describe each and every element of the claim, and the rejection should be withdrawn.

Without addressing the merits of the comments made in the Office Action with respect to claim 13, which are not specifically conceded, it is noted that claim 13 depends from claim 12 and includes all of its limitations. The arguments made above with respect to claim 12 apply equally to claim 13 and are herein incorporated. Therefore, claim 13 is allowable on the same basis as claim 12 by virtue of claim dependency, and the rejection should be withdrawn.

Rejections on Bude

Claims 1-7, 12 and 13 also stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 5,838,617 to Bude et al. (hereafter "Bude"). This rejection is respectfully traversed.

As was discussed above, claim 1 recites a method for programming a memory cell where hot carriers are injected into and stored on at least one charge storage dielectric layer from a drain side of the memory cell, where the at least one charge storage dielectric layer is included in a dielectric stack of a control gate. Bude does not disclose or describe such an approach.

In similar fashion as Lin, which was discussed above, Bude is directed to methods of programming floating gate memory devices. Such a floating gate memory device is illustrated in Figure 1 of Bude, which is included below for the Examiner's convenience.

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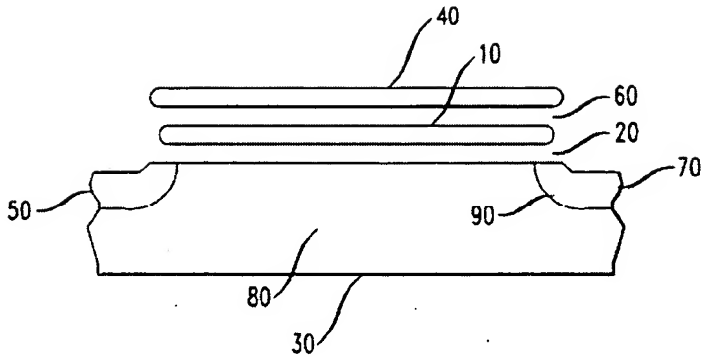

Figure 1

The floating gate memory device in Bude's Figure 1 includes a conductive floating gate electrode 10 (See column 3, lines 40-42). The floating gate memory device of Bude, in like fashion as Lin, is programmed by injecting hot carriers into the floating gate electrode 10 and storing the injected hot carriers in the floating gate electrode 10. (See column 3, line 31-35). Such a method does not disclose or describe a method of programming a memory device that includes injecting hot carriers into a charge storage dielectric layer and storing the injected carriers in the charge storage dielectric layer. Therefore, claim 1 is not anticipated by Bude because that patent fails to disclose or describe each and every element of the claim, and the rejection should be withdrawn.

Without addressing the merits of the comments made in the Office Action with respect to claims 2-7, which are not specifically conceded, it is noted that these claims depend from claim 1 and include all of its limitations and the limitations of any intervening claims. The arguments made above with respect to claim 1 apply equally to claims 2-7 and are herein incorporated. Therefore, claims 2-7 are allowable over Bude on the same basis as claim 1 by virtue of claim dependency, and the rejection should be withdrawn.

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As was discussed above with respect to Lin, claim 12 is directed to a memory circuit that includes an array of memory cells. The memory cells of the circuit of claim 12 are programmed as a result of hot carriers being injected, from a drain side of a memory cell, into and stored on at least one charge storage dielectric layer. In the memory cells, the at least one charge storage dielectric layer is included in a dielectric stack of a control gate. Bude does not disclose or describe such an approach.

As was also discussed above, Bude discloses floating gate memory circuits that are programmed by injecting hot carriers into a conductive floating gate electrode and storing the hot carriers on the floating gate electrode. In contrast, claim 12 recites a memory circuit including an array of memory cells that are programmed by injecting hot carriers into at least one charge storage dielectric layer and storing those injected hot carriers on the at least one charge storage dielectric layer. Thus, claim 12 is not anticipated by Bude as that patent does not disclose or describe each and every element of the claim, and the rejection should be withdrawn.

Without addressing the merits of the comments made in the Office Action with respect to claim 13, which are not specifically conceded, it is noted that claim 13 depends from claim 12 and includes all of its limitations. The arguments made above with respect to claim 12 apply equally to claim 13 and are herein incorporated. Therefore, claim 13 is allowable on the same basis as claim 12 by virtue of claim dependency, and the rejection should be withdrawn.

Allowable Subject Matter

Claims 14 and 16 are indicated as being allowable. Applicants respectfully thank the Examiner of this indication of allowability.

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Conclusion

In view of the foregoing, all of the pending claims are in condition for allowance. If the Examiner has any questions, he is invited to contact the undersigned at (360) 379-6514. An early allowance of all the claims is respectfully requested.

Respectfully Submitted,

McDonnell Boehnen Hulbert & Berghoff LLP

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CERTIFICATE OF MAILING UNDER 37 C.F.R. § 1.8

The undersigned hereby certifies that the foregoing RESPONSE TO OFFICE ACTION MAILED ON AUGUST 12, 2005 is being deposited as first class mail, postage prepaid, in an envelope addressed to Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 7 day of November 2005.

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